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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,514	03/28/2001	William C. Anderson	10559-394001	5444

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	4

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,514	ANDERSON ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/27/02* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "110" (page 3, line 17). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: at page 2, line 15, "102" should read -206-. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Roth et al. (PUB. No. US 2002/0078326 A1).

Referring to claim 1, Roth et al. discloses as claimed a method for use in a pipelined processor (see Fig. 2) including a plurality of stages (12, IF; 14 Decode; 18, AC; EX., 22 A-N; and WB, 30, see Fig. 2), the method comprising: storing a first updated data address value in a future file (34A, 34B, and 34C see Fig. 2); and generating (by Data Address Generator 19 see Fig. 2) a second data address value from said first updated data address value.

Referring to claim 8, Roth et al. discloses as claimed an article comprising a machine-readable medium (inherently existing in Roth et al.'s main memory) which stores machine-executable instructions, the instructions causing a machine to store a first updated data address value in a future file (34A, 34B, and 34C see Fig. 2); and generate (by Data

Address Generator 19 see Fig. 2) a second data address value from said first updated data address value.

Referring to claims 15 and 22, Roth et al. discloses as claimed a processor (inherently, the CPU of Roth et al.'s system) comprising: a pipeline comprising two or more stages (12, IF; 14 Decode; 18, AC; EX., 22 A-N; and WB, 30, see Fig. 2); a future file (34A, 34B, and 34C see Fig. 2) operative to store a first updated data address value; a data address generator (Data Address Generator 19 see Fig. 2) operative to generate a second updated data address value from said first updated data address value, and an update bus connected between the data address generator (Data Address Generator 19 see Fig. 2) and the future file (34A, 34B, and 34C see Fig. 2) and operative to write the second updated data address value to the future file (see Fig. 8, the second data address inside the counters in stages Ex.1- Ex. n-1 being sent back to a Multiplexer or selector and stored in 34C). Regarding claim 22, Roth et al. also discloses: a processor coupled to a static random access memory (Roth et al.'s main memory which is inherently existing).

As to claims 2 and 9, Roth et al. also discloses: storing said second data address value in the future file (see Fig. 8, the second data address inside the counters in stages Ex.1- Ex.

n-1 being sent back to a Multiplexer or selector and stored in 34C).

As to claims 3, 10, 18, and 25, Roth et al. also discloses: storing a committed data address value in an architectural file (32A-C, see Fig. 2 and left Col. at page 2, lines 5-10).

As to claims 4, and 11, Roth et al. also discloses: cancelling an instruction in the pipeline (when the speculation is not correct and need to be adjusted, see also left Col. at page 5, lines 5-7); and restoring the future file to a valid state by writing the committed data address value in the architectural file (32A-C, see Fig. 2 and left Col. at page 2, lines 5-10) to the future file (34A, 34B, and 34C see Fig. 2).

As to claims 5 and 12, Roth et al. also discloses: generating the second updated data address value comprises calculating the second updated data address value with a data address generator (Data Address Generator 19 see Fig. 2) in an address calculation stage (AC stage 18, see Fig. 2) of the pipeline.

As to claims 6 and 13, Roth et al. also discloses: providing the future file (34A, see Fig. 2) in a decode stage (Decode stage 14, see Fig. 2)of the pipeline.

As to claims 7, 14, 20, and 27, Roth et al. also discloses: storing the first updated data address value comprises storing

at least one of an index value (inherently exist in a data registers 34A-C), a length value, a base value, and a modify value in the future file (34A, 34B, and 34C see Fig. 2).

As to claims 16 and 23, Roth et al. also discloses: said two or more stages include a decode stage, an address calculation stage, an execution stage, and a write back stage (the stages 12, IF; 14 Decode; 18, AC; EX., 22 A-N; and WB, 30, see Fig. 2).

As to claims 17 and 24, Roth et al. also discloses: the future file (including 34a and 34b, see Fig. 2) is located in the decode stage (Decode stage 14, see Fig. 2) and the data address generator (Data Address Generator 19 see Fig. 2) is located in the address calculation stage (AC stage 18, see Fig. 2).

As to claims 19 and 26, Roth et al. also discloses: a restore bus (inherently existing in the Roth et al.'s system) connected between the architectural file and the future file; and a control unit (inherently existing in the CPU of the Roth et al.'s system) operative to write the committed data address values from the architectural file to the future file via the restore bus in response to the pipeline being cancelled (when the speculation is not correct and need to be adjusted, see also left Col. at page 5, lines 5-7).

As to claims 21 and 28, Roth et al. also discloses: the processor (the Roth et al.'s CPU, inherently existing) comprising a digital signal processor (note the Roth et al.'s processor is inherently a digital signal processor since it processes digital signals).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Clift et al. teaches a processor having primary array and shadow array for updating or restoring the register uses; Cherabuddi also teaches using working registers to handle the speculative data; and Liptay teaches ACL, DRAL, and BRAL for precise post-branch recoveries.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful,

the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

7. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into

the Group at fax number: 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
April 5, 2004